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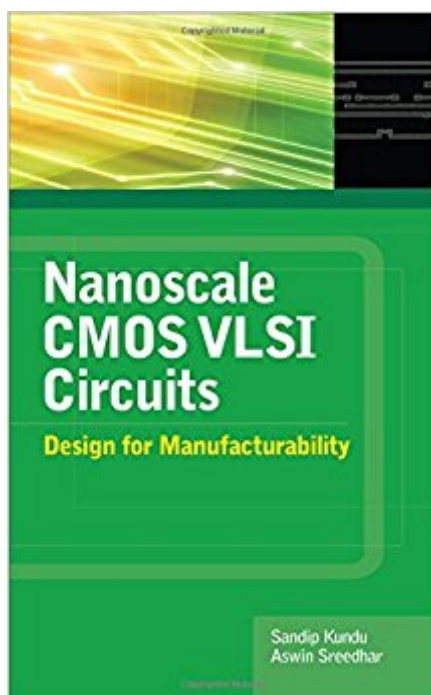
Nanoscale CMOS VLSI Circuits: Design For Manufacturability

Nanoscale CMOS VLSI Circuits
Design for Manufacturability

Sandip Kundu
Aswin Sreedhar

Synopsis

Cutting-Edge CMOS VLSI Design for Manufacturability Techniques This detailed guide offers proven methods for optimizing circuit designs to increase the yield, reliability, and manufacturability of products and mitigate defects and failure. Covering the latest devices, technologies, and processes, Nanoscale CMOS VLSI Circuits: Design for Manufacturability focuses on delivering higher performance and lower power consumption. Costs, constraints, and computational efficiencies are also discussed in the practical resource. Nanoscale CMOS VLSI Circuits covers: Current trends in CMOS VLSI design Semiconductor manufacturing technologies Photolithography Process and device variability: analyses and modeling Manufacturing-Aware Physical Design Closure Metrology, manufacturing defects, and defect extraction Defect impact modeling and yield improvement techniques Physical design and reliability DFM tools and methodologies

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Dr. Sandip Kundu is a professor in the Electrical and Computer Engineering Department at the University of Massachusetts at Amherst, specializing in semiconductor and lithographic manufacturing.Dr. Aswin Sreedhar is a research assistant at the Electrical and Computer Engineering Department at the University of Massachusetts.

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